

**AMENDMENTS TO THE CLAIMS**

**This listing of claims will replace all prior versions and listings of claims in the application:**

**LISTING OF CLAIMS:**

Claims 1-15. canceled

16. (currently amended): A semiconductor integrated circuit comprising:  
a plurality of analog/digital converting circuits operated in parallel for sequentially  
converting an analog image signal to a digital image signal;  
a multi-phase clock signal generating circuit for generating multi-phase clock signals to  
be used for periodically operating said plurality of analog/digital converting circuits in a certain  
order; and  
a control circuit for controlling said multi-phase clock signal generating circuit to change  
at least one of a period and an order of operating said plurality of analog/digital converting  
circuits in response to at least a synchronization signal which corresponds to the analog image  
signal.

17. (currently amended): ~~The semiconductor integrated circuit according to claim 16~~  
A semiconductor integrated circuit comprising:

a plurality of analog/digital converting circuits operated in parallel for sequentially  
converting an analog image signal to a digital image signal;  
a multi-phase clock signal generating circuit for generating multi-phase clock signals to  
be used for periodically operating said plurality of analog/digital converting circuits in a certain  
order; and  
a control circuit for controlling said multi-phase clock signal generating circuit to change  
at least one of a period and an order of operating said plurality of analog/digital converting  
circuits,

wherein said control circuit controls said multi-phase clock signal generating circuit  
based on a number of pixels included in one frame of the digital image signal and a number of

said plurality of analog/digital converting circuits such that said plurality of analog/digital converting circuits never performs conversion in a same period and in a same order with respect to pixels for at least successive two frames.

18. (previously presented): The semiconductor integrated circuit according to claim 17, wherein said control circuit controls said multi-phase clock signal generating circuit based on the number of pixels included in one frame of the digital image signal and the number of said plurality of analog/digital converting circuits such that said plurality of analog/digital converting circuits never performs conversion in a same period and in a same order with respect to pixels for successive N frames where the number of said plurality of analog/digital converting circuits is N.

19. (previously presented): The semiconductor integrated circuit according to claim 16, wherein said control circuit controls said multi-phase clock signal generating circuit based on an output of a pseudorandom number generating circuit for generating at least N integers where the number of said plurality of analog/digital converting circuits is N so as to shift timing of sampling operation of said plurality of analog/digital converting circuits.

20. (currently amended): ~~The semiconductor integrated circuit according to claim 16~~  
A semiconductor integrated circuit comprising:

a plurality of analog/digital converting circuits operated in parallel for sequentially converting an analog image signal to a digital image signal;

a multi-phase clock signal generating circuit for generating multi-phase clock signals to be used for periodically operating said plurality of analog/digital converting circuits in a certain order; and

a control circuit for controlling said multi-phase clock signal generating circuit to change at least one of a period and an order of operating said plurality of analog/digital converting circuits,

wherein said multi-phase clock signal generating circuit counts pulses of a master clock signal and stores counter values to be used for generating the multi-phase clock signals; and

said control circuit controls said multi-phase clock signal generating circuit by changing the counter values stored in said multi-phase clock signal generating circuit at predetermined timing.

21. (currently amended): ~~The semiconductor integrated circuit according to claim 16~~  
A semiconductor integrated circuit comprising:

a plurality of analog/digital converting circuits operated in parallel for sequentially converting an analog image signal to a digital image signal;

a multi-phase clock signal generating circuit for generating multi-phase clock signals to be used for periodically operating said plurality of analog/digital converting circuits in a certain order; and

a control circuit for controlling said multi-phase clock signal generating circuit to change at least one of a period and an order of operating said plurality of analog/digital converting circuits,

wherein said multi-phase clock signal generating circuit counts pulses of a master clock signal and stores counter values to be used for generating the multi-phase clock signals; and

said control circuit controls said multi-phase clock signal generating circuit by changing the counter values stored in said multi-phase clock signal generating circuit at predetermined timing based on a counter value obtained by counting the pulses of the master clock signal.

22. (currently amended): ~~The semiconductor integrated circuit according to claim 16~~  
A semiconductor integrated circuit comprising:

a plurality of analog/digital converting circuits operated in parallel for sequentially converting an analog image signal to a digital image signal;

a multi-phase clock signal generating circuit for generating multi-phase clock signals to be used for periodically operating said plurality of analog/digital converting circuits in a certain order; and

a control circuit for controlling said multi-phase clock signal generating circuit to change at least one of a period and an order of operating said plurality of analog/digital converting circuits,

wherein said control circuit outputs a clock signal obtained by suppressing a predetermined number of pulses included in a master clock signal; and

    said multi-phase clock signal generating circuit generates said multi-phase clock signals based on counter values obtained by counting pulses of the clock signal outputted from said control circuit.

23. (previously presented): The semiconductor integrated circuit according to claim 22, wherein said control circuit outputs the clock signal obtained by suppressing the predetermined number of pluses included in the master clock signal in a blanking period of the digital image signal.

24. (currently amended): A semiconductor integrated circuit comprising:  
    an analog/digital converting circuit for converting an analog image signal to a digital image signal by sequentially switching between a plurality of circuit elements;  
    a first control circuit for controlling said analog/digital converting circuit to periodically arrange said plurality of circuit elements in a certain order; and  
    a second control circuit for controlling said first control circuit to change at least one of a period and an order of arranging said plurality of circuit elements in response to at least a synchronization signal which corresponds to the analog image signal.

25. (currently amended): ~~The semiconductor integrated circuit according to claim 24~~  
A semiconductor integrated circuit comprising:  
    an analog/digital converting circuit for converting an analog image signal to a digital image signal by sequentially switching between a plurality of circuit elements;  
    a first control circuit for controlling said analog/digital converting circuit to periodically arrange said plurality of circuit elements in a certain order; and  
    a second control circuit for controlling said first control circuit to change at least one of a period and an order of arranging said plurality of circuit elements,

    wherein said second control circuit controls said first control circuit based on a number of pixels included in one frame of the digital image signal and a number of said plurality of circuit elements such that said analog/digital converting circuit never arranges said plurality of circuit

elements in a same period and in a same order with respect to pixels for at least successive two frames.

26. (currently amended): ~~The semiconductor integrated circuit according to claim 10~~

A semiconductor integrated circuit comprising:

an analog/digital converting circuit for converting an analog image signal to a digital image signal by sequentially switching between a plurality of circuit elements;

a first control circuit for controlling said analog/digital converting circuit to periodically arrange said plurality of circuit elements in a certain order; and

a second control circuit for controlling said first control circuit to change at least one of a period and an order of arranging said plurality of circuit elements,

wherein said second control circuit controls said first control circuit based on the number of pixels included in one frame of the digital image signal and the number of said plurality of circuit elements such that said analog/digital converting circuit never arranges said plurality of circuit elements in the same period and in the same order with respect to pixels for successive N frames where a number of said circuit elements is N.

27. (currently amended): ~~The semiconductor integrated circuit according to claim 24~~

A semiconductor integrated circuit comprising:

an analog/digital converting circuit for converting an analog image signal to a digital image signal by sequentially switching between a plurality of circuit elements;

a first control circuit for controlling said analog/digital converting circuit to periodically arrange said plurality of circuit elements in a certain order; and

a second control circuit for controlling said first control circuit to change at least one of a period and an order of arranging said plurality of circuit elements,

wherein said first control circuit counts a master clock signal and stores counter values to be used for generating multi-phase control signals for controlling said analog/digital converting circuit; and

    said second control circuit controls said first control circuit by changing the counter values stored in said first control circuit at predetermined timing.

28. (currently amended): ~~The semiconductor integrated circuit according to claim 24 A~~  
semiconductor integrated circuit comprising:

an analog/digital converting circuit for converting an analog image signal to a digital image signal by sequentially switching between a plurality of circuit elements;

a first control circuit for controlling said analog/digital converting circuit to periodically arrange said plurality of circuit elements in a certain order; and

a second control circuit for controlling said first control circuit to change at least one of a period and an order of arranging said plurality of circuit elements,

wherein said first control circuit counts a master clock signal and stores counter values to be used for generating multi-phase control signals for controlling said analog/digital converting circuit; and

    said second control circuit controls said first control circuit by changing the counter values stored in said first control circuit at a predetermined interval based on a counter value obtained by counting a master clock signal.

29. (currently amended): ~~The semiconductor integrated circuit according to claim 24 A~~  
semiconductor integrated circuit comprising:

an analog/digital converting circuit for converting an analog image signal to a digital image signal by sequentially switching between a plurality of circuit elements;

a first control circuit for controlling said analog/digital converting circuit to periodically arrange said plurality of circuit elements in a certain order; and

a second control circuit for controlling said first control circuit to change at least one of a period and an order of arranging said plurality of circuit elements,

wherein said second control circuit outputs a clock signal obtained by suppressing a predetermined number of pulses included in a master clock signal; and

    said first control circuit generates multi-phase control signals for controlling said analog/digital converting circuit based on counter values obtained by counting the clock signal outputted from said second control circuit.

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30. (previously presented): The semiconductor integrated circuit according to claim 28, wherein said second control circuit outputs the clock signal obtained by suppressing the predetermined number of pulses included in the master clock signal in a blanking period of the digital image signals.